AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of claims:

1. (ORIGINAL) A method of fabrication of a bond pad structure, comprising the steps of:

a) providing a top wiring layer and a top dielectric layer over a semiconductor structure;

b) forming a buffer dielectric layer over said top wiring layer and said top dielectric layer;

c) forming a buffer opening in said buffer dielectric layer exposing at least of portion of said top wiring layer;

d) forming a barrier layer over said buffer dielectric layer, and said top wiring layer in said buffer opening;

e) forming a conductive buffer layer over said barrier layer;

f) planarizing said conductive buffer layer to form a buffer pad in said buffer opening;

g) forming a passivation layer over said buffer pad and said buffer dielectric layer;

h) forming a bond pad opening in said passivation layer over at least a portion of said buffer pad;

i) forming a bond pad support layer over said buffer pad and passivation layer;

j) forming a bond pad layer over said bond pad support layer;

k) patterning said bond pad layer and said bond pad support layer to form a bond pad and bond pad support.

2. (ORIGINAL) The method of claim 1 wherein said top wiring layer is comprised of Cu alloy; said top wiring layer is a damascene interconnect.

3. (ORIGINAL) The method of claim 1 wherein said top dielectric layer is comprised of oxide made from tetraethylorthosilicate (TEOS) reactants and has a thickness between 6750 and 8250 Å.

4. (CANCELED)

5. (ORIGINAL) The method of claim 1 wherein said top dielectric layer is comprised an oxide based low k dielectric material with a K equal or less than 3.0.

6. (ORIGINAL) The method of claim 1 wherein said buffer dielectric layer is comprised of TEOS oxide and has a thickness between 6750 and 8250 Å.

7. (ORIGINAL) The method of claim 1 wherein said barrier layer is comprised of Ta or a bilayer comprised of a Cr layer and a Cr-Cu layer; said barrier layer has a thickness between 360 and 440 Å.

8. (CURRENTLY AMENDED) The method of claim 1 wherein said ~~conductive~~ buffer pad ~~layer~~ is comprised of an aluminum alloy with between a 99.45 and 99.55 wt

% aluminum and between 0.45 and 0.55 wt % copper. ~~; said conductive buffer layer has a thickness between 6750 and 8250 Å.~~

9. (ORIGINAL) The method of claim 1 wherein the planarization of said conductive buffer layer comprises a chemical-mechanical polish step.

10. (ORIGINAL.) The method of claim 1 wherein said passivation layer is comprised of a three layer structure of (1) lower silicon nitride layer , (2) undoped silicate glass layer and (3) upper silicon nitride layer; and has a thickness between 13500 and 16500 Å.

11. (ORIGINAL) The method of claim 1 wherein said bond pad opening has an area between 2500 and 10000 sq μm.

12. (ORIGINAL.) The method of claim 1 wherein said buffer opening is larger than said bond pad opening; said buffer opening extends beyond said bond pad opening on all sides.

13. (ORIGINAL) The method of claim 1 wherein said bond pad support layer is comprised of a material selected from the group consisting of Ti, TiW, W and Cr; and has thickness between 2000 and 6000 Å.

14. (ORIGINAL) The method of claim 1 wherein said bond pad layer comprised of an Al-Cu alloy with Al between 99.45 and 99. 55 wt % and Cu between 0.45 and 0.55 % ; said bond pad layer has a thickness between 6000 and 15000 Å; and said buffer pad underlies the entire bond pad.

15. (ORIGINAL) The method of claim 1 wherein said buffer pad underlies the entire bond pad; said buffer pad has a larger area than said bond pad by between 10 % and 30 % of the area of the bonding pad.

16. (CANCELED)

17. (ORIGINAL) A bond pad structure comprising:

a) a top wiring layer and a top dielectric layer over a semiconductor structure;

b) a buffer dielectric layer over said top wiring layer and said top dielectric layer;

c) a buffer opening in said buffer dielectric layer exposing at least of portion of said top wiring layer;

d) a buffer pad over said buffer dielectric layer and said top wiring layer in said buffer opening;

e) forming a passivation layer over said conductive buffer pad and said buffer dielectric layer;

f) a bond pad opening in said passivation layer over at least a portion of said buffer pad

g) a bond pad and bond pad support over said passivation layer over at least a portion of said buffer pad. in at least said bond pad opening.

18. (ORIGINAL) The bond pad structure of claim 17 wherein said top wiring layer is comprised of Cu alloy; said top wiring layer is a damascene interconnect

19. (ORIGINAL) The bond pad structure of claim 17 wherein said top dielectric layer is comprised of TEOS oxide and has a thickness between 6750 and 8250 Å.

20. (ORIGINAL) The bond pad structure of claim 17 said top dielectric layer is comprised black diamond ™ film.

21. (ORIGINAL) The bond pad structure of claim 17 said top dielectric layer is comprised an oxide based low k dielectric material with a K equal or less than 3.0.

22. (ORIGINAL) The bond pad structure of claim 17 wherein said barrier layer is comprised of Ta or a bilayer comprised of a Cr layer and a Cr-Cu layer; said barrier layer has a thickness between 360 and 440 Å.

23. (ORIGINAL) The bond pad structure of claim 17 wherein said conductive buffer layer is comprised of an Aluminum alloy with between a 99.45 and 99. 55 wt % Aluminum and between 0.45 and 0.55 wt % copper; said conductive buffer layer has a thickness between 6750 and 8250 Å.

24. (ORIGINAL) The bond pad structure of claim 17 wherein said passivation layer is comprised of a three layer structure of (1) lower silicon nitride layer, (2) undoped silicate glass layer and (3) upper silicon nitride layer; and has a thickness between 13500 and 16500 Å.

25. (ORIGINAL) The bond pad structure of claim 17 wherein said bond pad support layer is comprised of a material selected from the group consisting of Ti or TiW, and Cr; and has thickness between 2000 and 6000 Å.

26. (ORIGINAL) The bond pad structure of claim 17 wherein said bond pad layer comprised of an Al-Cu alloy and said bond pad layer has a thickness between 6000 and 15000 Å; and said buffer pad underlies the entire bond pad.

27. (ORIGINAL.) The bond pad structure of claim 17 wherein said buffer pad underlies the entire bond pad; said buffer pad has a larger area than said bond pad by between 10 % and 30 % of the area of the bonding pad.

28. (NEW) A method of fabrication of a bond pad structure, comprising the steps of:

providing a top wiring layer and a top dielectric layer over a semiconductor structure;

forming a buffer dielectric layer over said top wiring layer and said top dielectric layer;

forming a buffer opening in said buffer dielectric layer exposing at least of portion of said top wiring layer;

forming a buffer pad in said buffer opening;

forming a passivation layer over said buffer pad and said buffer dielectric layer;

forming a bond pad opening in said passivation layer over at least a portion of said buffer pad;

forming a bond pad and bond pad support at least in said bond pad opening.